REMARKS

Status of Claims:

Claims 1-10 are present for examination.

Prior Art Rejection:

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of Duvvury (5,814,865).

The Examiners rejection is respectfully traversed.

On page 3 of the Office Action, the Examiner stated in connection with figure 2 of Duvvury as follows.

> "Duvvury et al. teach in figure 2 and related text a first conductive well 204 formed directly **under the first source diffusion layer 212** and thereby the first conductive type well is electrically connected directly with the source diffusion layer, and underlies a dopant diffusion region of the second conductivity type 210, and having a lower dopant concentration than the first diffusion layer." (Emphasis added.)

However, the Examiner has left out important relevant portions of the Duvvury description.

The more complete and exact description of Duvvury stated as follows. (See lines 17-30 column 4.)

> "The second nMos device is defined by source/drain regions 212 and 214 and conductive gate structure 216. As with the first nMos device, source/drain regions 212 and 214 are preferably n^+ regions and conductive gate structure 216 is connected to **source region 214** via contacts 226 and 228. In addition, contacts 226 and 228 are connected to ground. Lightly doped region 204 is situated between the two nMos

> devices, and heavily doped region 210 is situated within region 204. Preferably, lightly doped region is an n^- region 204 and heavily doped region 210 is a p^+ region." (Emphasis added.)

Thus, the description clearly teaches the second nMos device having the **source region 214** and **drain region 212**, where lightly doped region 204 is formed directly under the **drain region 212** and thereby the first conductive type well 204 is electrically connected directly with the **drain region 212**. In addition, **the conductive gate structure 216 is connected to the source region 214** via contacts 226 and 228.

It seems clear that the Examiner has misinterpreted Duvvury based on portions of the Duvvury description which state "source/drain regions 212 and 214". However, as made clear by the more complete excerpts of the patent set forth above, the source region is not region 212 but rather region 214. Moreover, the drain region is not region 214 but rather region 212. Thus, while Duvvury apparently causes come confusion, the further explanation makes it quite clear that region 214 is the source region and region 212 is the drain region. Further support for this conclusion is based on the description of figure 2(a) as may be seen by the below quotations.

Duvvury stated:

> "Due to the placement of regions 208, 210, 212, a diode is termed by region 210 and 208 and another diode is formed by regions 210 and 212. Since these two diodes are in parallel, they, as a pair, will have a lower resistance." (See line 27-31 column 4.)

> "More specifically, the circuit of Fig. 2a Illustrates the device of Fig. 2 where terminals 220, 222, 224, 226, and 228 are all connected to V_{ss} (represented by block 238, and is preferably grounded) and terminals 223 and 225 are connected to V_{pp} (represented in Fig. 2a as block 230)." (See lines 40-44, column 4.)

Accordingly, Duvvury teaches such a diode structure termed by the heavily doped p^+ region 210 and the **drain region 212**, where the heavily doped p^+ region 210 and the **source region 214** are connected to V_{ss}, respectively, via terminals 224 and 228, whereas the **drain region 212** is connected to V_{pp} via terminal 225.

Duvvury clearly teaches a structure in which the heavily doped p^+ region 210 is situated within the lightly doped (n^-) region 204 so as to build up $p^+/n^-/n^+$ type junction for the diode (234) formed by the heavily doped p^+ region 210 and the drain region 212.

In contrast, in N-channel MOSFET claimed in claim 1, the current path from the n^+ drain region 3b to the p^+ dopant diffusion region 4a has a $p^+/p^-/n^+$ type junction by using the p^- well 2.

Moreover, even if the Duvvury structure of a first conductive type well 204 being formed directly under the **drain region 212** is applied to the semiconductor device shown in figure 7 (APA), the resulted semiconductor device is clearly far different from the semiconductor device of the present invention as claimed in claim 1.

Conclusions:

It is submitted that applicant's claims already clearly distinguish applicant's invention from the combined teachings of APA and Duvvury. As such, the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. § 103.

It is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of

papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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